

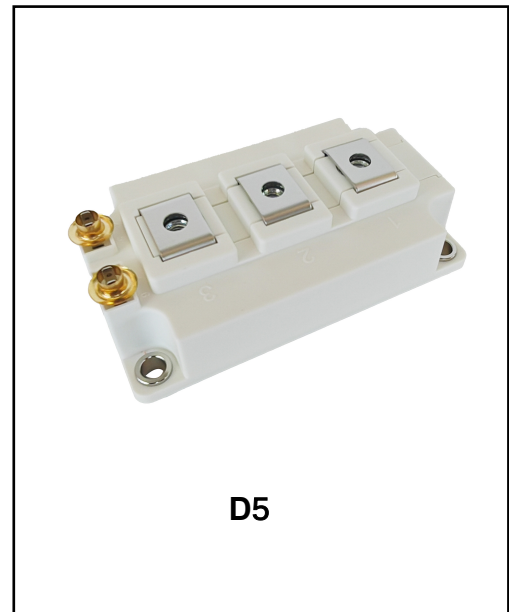
D5 module with Trench/Fieldstop IGBT and Emitter Controlled diode

Features

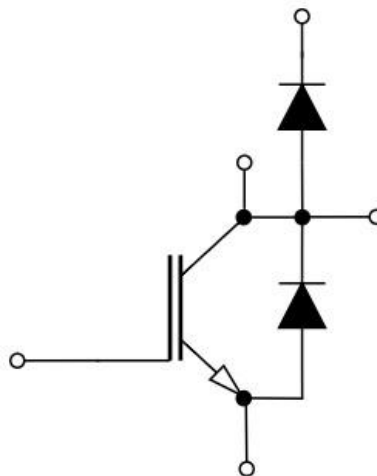
- Low $V_{CE(sat)}$ Trench IGBT technology
- High creepage and clearance distances
- $V_{CE(sat)}$ with positive temperature coefficient
- Maximum junction temperature 175°C
- Package with CTI>400

Typical Applications

- 3-level-applications
- Motor Drives
- Chopper application



Description



Package Insulation coordination

Parameter	Symbol	Note or test condition	Values	Unit
Isolation test voltage	V_{ISOL}	RMS, f=50 Hz, t=60 s	4.0	kV
Internal isolation		basic insulation(class 1, IEC 61140)	Al_2O_3	
Creepage distance	d_{creep}	terminal to heatsink	29.0	mm
Creepage distance	d_{creep}	terminal to terminal	23.0	mm
Clearance	d_{clear}	terminal to heatsink	23.0	mm
Clearance	d_{clear}	terminal to terminal	11.0	mm
Comparative tracking index (electrical)	CTI		>400	

Package Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Stray Inductance	L_{CE}			--	20	--	nH
Module Lead Resistance, Terminal to Chip	R_{CC+EE}			--	0.70	--	mΩ
Storage temperature	T_{stg}			-40	--	125	°C
Mounting torque for module mounting	M	-Mounting according to valid application note	M6, Screw	3.00	--	6.00	Nm
Terminal connection torque	M	-Mounting according to valid application note	M6, Screw	2.5	--	5.0	Nm
Weight	G			--	340	--	g

IGBT , Brake-Chopper

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Description	Value	Unit
V_{CES}	Collector-Emitter Voltage	1700	V
V_{GES}	Gate-Emitter Voltage	± 30	V
I_{CDC}	Continuous Collector Current @ $T_c = 80^\circ\text{C}$ ($T_{vj\max} = 175^\circ\text{C}$)	300	A
I_{CM}	Pulsed Collector Current, $t_p = 1\text{ ms}$	600	A
$T_{vj\max}$	Maximum Junction Temperature	175	$^\circ\text{C}$

Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V _{CE(sat)}	Collector–Emitter Saturation Voltage	I _C =300A, V _{GE} = 15V	T _{vj} = 25 °C	--	1.75	2.20	V
			T _{vj} = 150 °C	--	2.20	--	
V _{GE(TH)}	Gate–Emitter Threshold Voltage	I _C =12mA, V _{CE} =V _{GE}		4.80	5.40	6.50	V
I _{CES}	Collector–Emitter Cutoff Current	V _{GE} = 0 V, V _{CE} = 1700V		--	--	100	μA
I _{GES}	Gate-Emitter Leakage Current	V _{GE} = ±30 V, V _{CE} = 0 V, T _{vj} = 25°C		--	--	100	nA
R _{Gint}	Internal Gate Resistance	f=1MHz		--	4.37	--	Ω
C _{ies}	Input Capacitance	V _{CE} =25V, V _{GE} =0V, f=1MHz		--	12.5	--	nF
C _{res}	Reverse Transfer			--	0.21	--	nF
Q _G	Gate Charge	V _{CC} = 900 V, V _{GE} =15 V		--	1.05	--	μC
t _{d(on)}	Turn-On Delay Time	V _{CE} = 900 V, I _C =300 A, R _{Gon} = 10Ω, R _{Goff} = 15Ω V _{GE} =±15V Inductive Load T _{vj} = 25°C		--	0.40	--	μs
t _r	Rise Time			--	0.13	--	
t _{d(off)}	Turn-off Delay Time			--	1.36	--	
t _f	Fall Time			--	0.25	--	
E _{on}	Turn-On Switching Loss per Pulse			--	141.5	--	mJ
E _{off}	Turn Off Switching Loss per Pulse			--	83.8	--	
t _{d(on)}	Turn-On Delay Time	V _{CE} = 900 V, I _C =300 A, R _{Gon} = 10Ω, R _{Goff} = 15Ω V _{GE} =±15V Inductive Load T _{vj} = 150°C		--	0.39	--	μs
t _r	Rise Time			--	0.17	--	
t _{d(off)}	Turn-off Delay Time			--	1.53	--	
t _f	Fall Time			--	0.45	--	
E _{on}	Turn-on Switching Loss per Pulse			--	194.4	--	mJ
E _{off}	Turn Off Switching Loss per Pulse			--	114.5	--	
I _{c(sc)}	SC Data	t _p ≤10 μs, V _{GE} ≤15 V, T _{vj} ≤150 °C, V _{CC} =1000 V, V _{CEmax} =V _{CES} -L _{SCE} ·di/dt		--	1259	--	A
R _{thJC}	Thermal resistance	Junction-to-Case (per IGBT)			0.120		K/W
T _{vj op}	Temperature under switching conditions			-40		175 ¹⁾	°C

¹⁾ $T_{vj\text{ op}} > 150^\circ\text{C}$ is only allowed for operation at overload conditions. For detailed specifications please refer to AN 2018-14.

Diode , Brake-Chopper

Absolute Maximum Ratings (T_c = 25°C unless otherwise noted)

Symbol	Description	Value	Unit
V _{RRM}	Repetitive Peak Reverse Voltage	1700	V
I _F	Diode Continuous Forward Current	300	A
I _{FM}	Diode Maximum Forward Current, t _p =1ms	600	A

Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _F	Diode Forward Voltage	I _F = 300 A, T _{vj} =25°C	--	1.60	2.10	V
		I _F =300 A, T _{vj} =150°C	--	1.75	--	
T _{rr}	Reverse Recovery Time	V _{CE} =900 V, V _{GE} =-15 V, I _F =300 A T _{vj} = 25°C	--	0.85	--	μs
I _{RM}	Peak Reverse Recovery Current		--	234	--	A
Q _{rr}	Recovered Charge		--	71	--	μC
E _{rec}	Reverse Recovery Energy		--	29.2	--	mJ
T _{rr}	Reverse Recovery Time	V _{CE} =900 V, V _{GE} = -15 V I _F =300 A T _{vj} = 150°C	--	1.39	--	ns
I _{RM}	Peak Reverse Recovery Current		--	221	--	A
Q _{rr}	Recovered Charge		--	117	--	μC
E _{rec}	Reverse Recovery Energy		--	54.3	--	mJ
R _{thJC}	Thermal resistance	Junction-to-Case (per diode)		0.180		K/W
T _{vj op}	Temperature under switching conditions		-40		175 ²⁾	°C

²⁾T_{vj op} > 150°C is only allowed for operation at overload conditions. For detailed specifications please refer to AN 2018-14.

Diode , Reverse

Absolute Maximum Ratings (T_c = 25°C unless otherwise noted)

Symbol	Description	Value	Unit
V _{RRM}	Repetitive Peak Reverse Voltage	1700	V
I _F	Diode Continuous Forward Current	300	A
I _{FM}	Diode Maximum Forward Current t _p =1ms	600	A

Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _F	Diode Forward Voltage	I _F = 300 A, T _{vj} = 25°C	--	1.60	2.10	V
		I _F = 300 A, T _{vj} = 175°C	--	1.75	--	
R _{thJC}	Thermal resistance	Junction-to-Case (per diode)	--	0.180		K/W
T _{vj op}	Temperature under switching conditions		-40		175 ³⁾	°C

³⁾T_{vj op} > 150°C is only allowed for operation at overload conditions. For detailed specifications please refer to AN 2018-14.

The diagram shows a 6-transistor CMOS circuit for a 3-input majority gate. The input nodes are labeled 1, 2, and 3. The output node is labeled 6. The circuit consists of a PMOS network (top) and an NMOS network (bottom). The PMOS network is a parallel combination of three series branches: (1) PMOS1 and PMOS2 in series, (2) PMOS3 and PMOS4 in series, and (3) PMOS5 and PMOS6 in series. The NMOS network is a series combination of three parallel branches: (1) NMOS1 and NMOS2 in parallel, (2) NMOS3 and NMOS4 in parallel, and (3) NMOS5 and NMOS6 in parallel. The output node 6 is connected to the PMOS network and the NMOS network. The input nodes 1, 2, and 3 are connected to the gates of the transistors. The output node 6 is connected to the drains of the PMOS transistors and the sources of the NMOS transistors. The source of PMOS6 and the source of NMOS6 are connected to ground (node 2).

Technical drawing of the top view of a mechanical part. The drawing shows a rectangular component with a central slot and four mounting holes. Dimensions are provided in millimeters with tolerances. Key dimensions include: overall width 106.4 ± 0.3, overall height 61.4 ± 0.3, central slot width 93 ± 0.2, and mounting hole diameter Ø1.5. Surface finish symbols are present on various surfaces.