

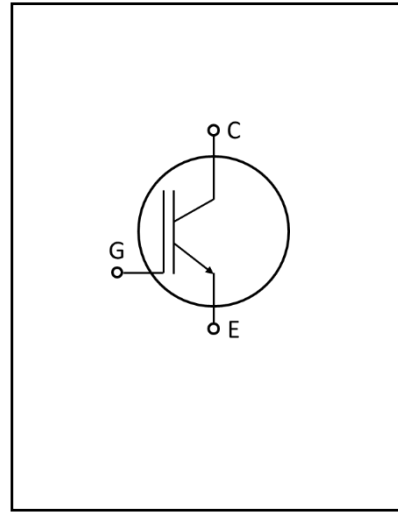
IGBT Chip

Features:

- 650V Trench & Field stop technology
- Low switching losses and V_{cesat}
- Positive temperature coefficient
- Easy paralleling

Applications:

- Photovoltaic
- Charging pile



Mechanical parameters

Die size	5.00×5.00	mm ²
Emitter pad size	See chip drawing	
Gate pad size	0.45×0.45	
Area total	25.00	
Thickness	70	μm
Wafer size	200	mm
Max. possible chips per wafer	1081	
Passivation front side	Polyimide	
Pad metal	AlCu with Ti/TiN (5μm & 200A/700A)	
Backside metal	AlSi/Ti/NiV/Ag	

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage	V_{CE}	650	V
DC collector current	I_C	75	A
Operating junction temperature	T_{vj}	-40 ... +175	°C
Gate emitter voltage	V_{GE}	±20	V

Static Characteristics (tested on wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}, I_C=1\text{mA}$	650			V
Collector-Emitter saturation voltage	V_{CEsat}	$V_{GE}=15\text{V}, I_C=75\text{A}$		1.61	1.90	
Gate-Emitter threshold voltage	$V_{GE(th)}$	$I_C=0.75\text{mA}, V_{GE}=V_{CE}$	4.7	5.3	5.9	
Zero gate voltage collector current	I_{CES}	$V_{CE}=650\text{V}, V_{GE}=0\text{V}$			10	μA
Gate-Emitter leakage current	I_{GES}	$V_{CE}=0\text{V}, V_{GE}=20\text{V}$			100	nA
Integrated gate resistor	$r_G^{a)}$			0		Ω
Input capacitance	$C_{ies}^{a)}$	$V_{CE}=25\text{V}, V_{GE}=0\text{V},$ $f=100\text{ kHz}$		4285		pF
Output capacitance	$C_{oes}^{a)}$			171		
Reverse transfer capacitance	$C_{res}^{a)}$			20		

Chip Drawing

