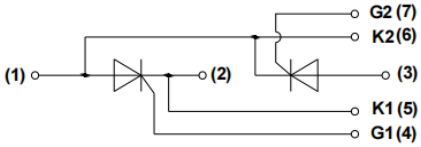
Description

1) A package of series of two chips.
2) With high thermal conductivity DBC as the insulation.
3) Welding by vacuum welding technology, which provide high reliability.



Typical Application

DC motor control, temperature control and light control system.

Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values	Unit
Operating junction temperature range		T_J	-40-125	℃
Storage temperature range		T_{STG}	-40-125	℃
Repetitive peak off-state voltage	T_J=25℃	V_{DRM}	2200	V
Repetitive peak reverse voltage	T_J=25℃	V_{RRM}	2200	V
Non-repetitive peak off-state voltage	T_J=25℃	V_{DSM}	2300	V
Non-repetitive peak reverse voltage	T_J=25℃	V_{RSM}	2300	V
Average on-state current	T_C=85℃	$I_{T(AV)}/I_{F(AV)}$	90	A
Peak on-state surge current	t_P=10ms V_R=0.6V_{RRM}	I_{TSM}/I_{FSM}	1800	A
I^2t value for fusing	t_P=10ms V_R=0.6V_{RRM}	I^2t	16200	A^2s
Critical rate of rise of on-state current	I_G=2×I_{GT}	di/dt	150	A/μs
Insulation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000	V

Electrical Characteristics (Packaged into modules, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	I_T=270A t_P=380μs	V_{TM}	≤1.8	V
Threshold voltage	T_J=125℃	V_{TO}	≤0.95	V
Dynamic resistance	T_J=125℃	R_d	≤2.1	mΩ
Repetitive peak off-state current	V_D=V_{DRM} T_C=25℃ T_C=125℃	 I_{DRM1} I_{DRM2}	 ≤100 ≤30	 μA mA
Repetitive peak reverse current	V_R=V_{RRM} T_C=25℃ T_C=125℃	 I_{RRM1} I_{RRM2}	 ≤100 ≤30	 μA mA
Triggering gate current	V_D=12V R_L=30Ω	I_{GT}	20-120	mA
Holding current	I_T=1A	I_H	≤250	mA
Latching current	I_G=1.2I_{GT}	I_L	≤300	mA
Triggering gate voltage	V_D=12V R_L=30Ω	V_{GT}	≤1.8	V
Non triggering gate voltage	V_D=V_{DRM} T_J=125℃	V_{GD}	≥0.25	V
Critical rate of rise of voltage	V_D=2/3V_{DRM} T_J=125℃ Gate Open	dv/dt	≥1000	V/μs
Thermal resistance	Junction to base plate Case to heatsink Junction to case	$R_{th(j-b)}$ $R_{th(c-s)}$ $R_{th(j-c)}$	0.34 0.22 0.30	℃/W

Performance Curves

FIG.1: Power dissipation vs. on-state current (per thyristor)

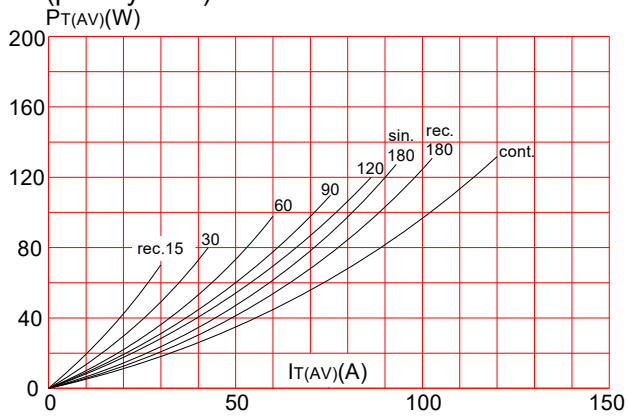


FIG.2: Maximum transient thermal impedance junction to case(per thyristor)

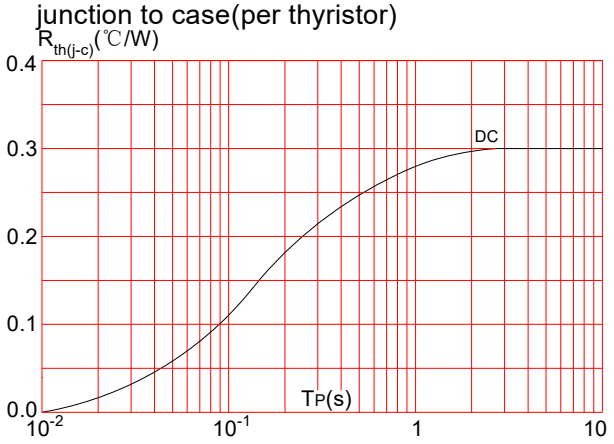


FIG.3: Forward characteristics (per thyristor)

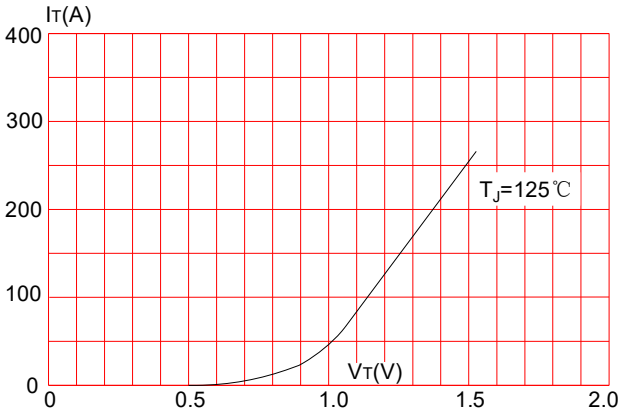
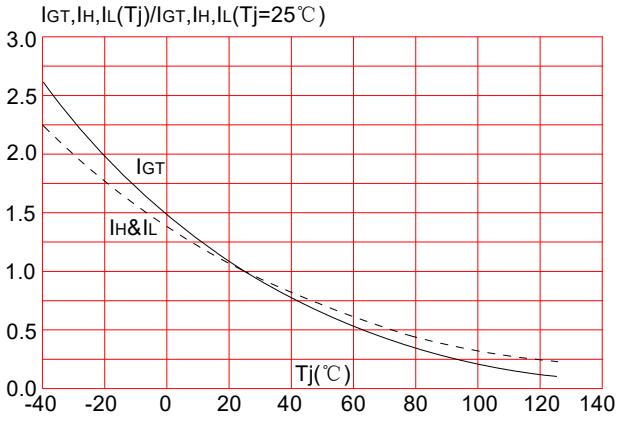
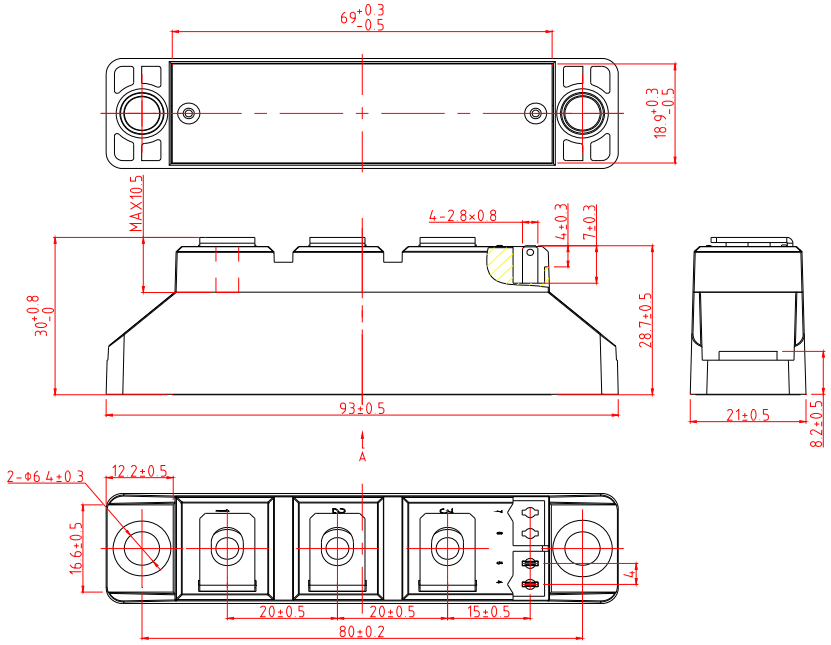


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature

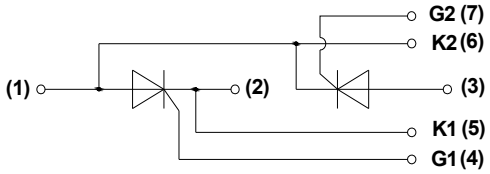


Mechanical Characteristics

Module size	93mm×21mm
Module height	30mm
Terminal distance of (1) /(2) /(3)	20mm
Mounting torque(M5)	5±15%Nm
Terminal torque(M5)	3±15%Nm



T1



symbol