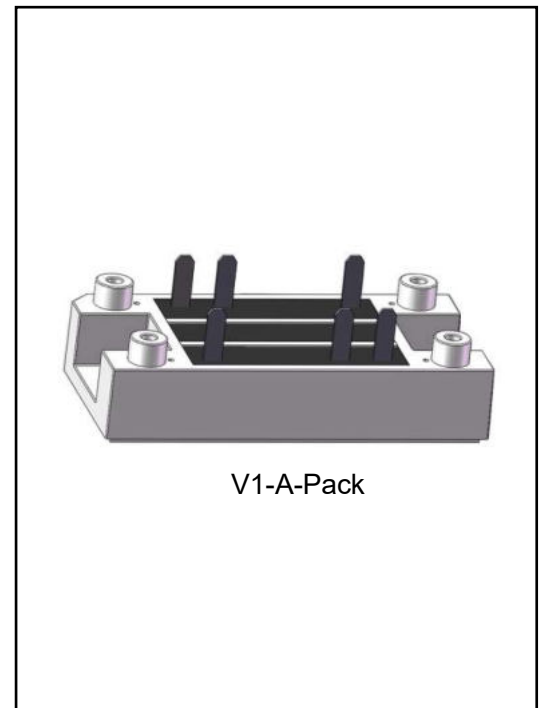


Anti-parallel Module

Description

- 1) A package consists of two inverse parallel SCR chips, which non-repetitive peak off-state voltage is up to 2300V
- 2) Welding by vacuum welding technology, which provides high reliability
- 3) Insulated by silicone gel, providing an insulation voltage of 3000V~



Typical Application

Soft start, solid state relay, AC/DC switch, temperature control.

Absolute Maximum Ratings (Packaged into V1-A-Pack, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

Parameter	Test Conditions	Symbol	Values			Unit
			18	20	22	
Operating junction temperature range		T_j	-40-125			$^{\circ}C$
Storage temperature range		T_{stg}	-40-125			$^{\circ}C$
Repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DRM}	1800	2000	2200	V
Repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RRM}	1800	2000	2200	V
Non-repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DSM}	1900	2100	2300	V
Non-repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RSM}	1900	2100	2300	V
RMS on-state current	$T_C=85^{\circ}C$	$I_{T(RMS)}$	120			A
Peak on-state surge current	$t_p=10ms$ $V_R=0.6V_{RRM}$	I_{TSM}	1200			A
I^2t value for fusing	$t_p=10ms$ $V_R=0.6V_{RRM}$	I^2t	7200			A^2s
Critical rate of rise of on-state current	$I_G=2 \times I_{GT}$	di/dt	150			$A/\mu s$
Insulation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000			V

Electrical Characteristics (Packaged into V1-A-Pack, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	$I_T=240A$ $t_p=380\mu s$	V_{TM}	≤ 1.8	V
Threshold voltage	$T_j=125^{\circ}C$	V_{TO}	≤ 0.95	V
Dynamic resistance	$T_j=125^{\circ}C$	R_d	≤ 2.1	m Ω
Repetitive peak off-state current	$V_D=V_{RRM}$ $T_C=25^{\circ}C$	I_{DRM1}	≤ 100	μA
	$T_C=125^{\circ}C$	I_{DRM2}	≤ 30	mA
Repetitive peak reverse current	$V_R=V_{RRM}$ $T_C=25^{\circ}C$	I_{RRM1}	≤ 100	μA
	$T_C=125^{\circ}C$	I_{RRM2}	≤ 30	mA
Triggering gate current	$V_D=12V$ $R_L=30\Omega$	I_{GT}	20-120	mA
Holding current	$I_T=1A$	I_H	≤ 250	mA
Latching current	$I_G=1.2 I_{GT}$	I_L	≤ 300	mA
Triggering gate voltage	$V_D=12V$ $R_L=30\Omega$	V_{GT}	≤ 1.8	V
Non triggering gate voltage	$V_D=V_{DRM}$ $T_j=125^{\circ}C$	V_{GD}	≥ 0.25	V
Critical rate of rise of voltage	$V_D=2/3V_{DRM}$ $T_j=125^{\circ}C$ Gate Open	dv/dt	≥ 1000	V/ μs
Thermal resistance	Junction to case	$R_{th(j-c)}$	0.37	$^{\circ}C/W$

Mechanical Characteristics

Module size	63x31.6mm					
Module height	21.6mm					
Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	2.85	3	3.15	0.112	0.118	0.124
B	2.3	2.5	2.7	0.091	0.098	0.106
C	1.9	2.1	2.3	0.075	0.083	0.091
D			6			0.236
E	16.25	17	17.75	0.640	0.669	0.699
F	0.4	0.5	0.6	0.016	0.020	0.024
G	20.85	21.6	22.35	0.821	0.850	0.880
H	30.85	31.6	32.35	1.215	1.244	1.274
I	23	23.5	24	0.906	0.925	0.945
J	0.25	0.75	1.25	0.010	0.030	0.049
K	10.5	11	11.5	0.413	0.433	0.453
L	6.5	7	7.5	0.256	0.276	0.295
M	49.5	50	50.5	1.949	1.989	1.988
N	51	51.5	52	2.008	2.028	2.047
O	62.25	63	63.75	2.451	2.480	2.510
P	10.25	11	11.75	0.404	0.433	0.463
Q	5.6	6.1	6.6	0.220	0.240	0.260
R	0.3	0.5	0.7	0.012	0.020	0.028
S	2.55	2.75	2.95	0.100	0.108	0.116
T	0.25	0.75	1.25	0.010	0.030	0.049
U	10.5	11	11.5	0.413	0.433	0.453
V	6.5	7	7.5	0.256	0.276	0.295
W	10.5	11	11.5	0.413	0.433	0.453

Ordering Information

Aiko Electronics Technology Co., LTD	<u>AK</u>	<u>121</u>	<u>KQ</u>	<u>-22</u>
		$I_{T(RMS)}=120A$		18: $V_{DSM}/V_{RSM} \geq 1900V$ 20: $V_{DSM}/V_{RSM} \geq 2100V$ 22: $V_{DSM}/V_{RSM} \geq 2300V$
			Module of anti-parallel of SCRs	